IN THE CLAIMS:

Please amend the claims as follows. The claims are in the format required by 35 C.F.R. § 1.121.

1. (Canceled)

2. (Previously presented) A system comprising:

a clock source;

a first counter coupled to receive a clock signal from the clock source and configured to count cycles of the clock signal in a sample period corresponding to a first digital data stream;

a second counter coupled to receive the clock signal from the clock source and configured to count cycles of the clock signal in a sample period corresponding to a second digital data stream; and

a data processor coupled to the first and second counters and configured to

read a first number of cycles counted by the first counter and a second number of cycles counted by the second counter, and

convert at least one of the first and second digital data streams from a corresponding input sample rate to a predetermined sample rate based on the number of cycles counted in the corresponding digital data stream,

wherein the first counter is configured to count cycles corresponding to the first digital data stream by incrementing once for each cycle after a frame sync signal is received in the first digital data stream and wherein the second counter is configured to count cycles corresponding to the second digital data stream by incrementing once for each cycle after a frame sync signal is received in the second digital data stream.

3-11. (Canceled)

12. (Previously presented) A method comprising:

receiving a clock signal from a clock source;

receiving a first digital data stream;

receiving a second digital data stream;

counting a first number of cycles of the clock signal in a sample period corresponding to a first digital data stream and a second number of cycles of the clock signal in a sample period corresponding to a second digital data stream, wherein counting the first number of cycles for the first digital data stream comprises incrementing a first counter once for each cycle after a frame sync signal is received in the first digital data stream and counting the second number of cycles for the second digital data stream comprises incrementing a second counter once for each cycle after a frame sync signal is received in the second digital data stream; and

converting at least one of the first and second digital data streams from a corresponding input sample rate to a predetermined sample rate based on the number of cycles counted for the corresponding digital data stream.

13. (Original) The method of claim 12, wherein counting the first number of cycles for the first digital data stream further comprises reading a first value from the first counter and wherein counting the second number of cycles for the second digital data stream further comprises reading a second value from the second counter.

14-21. (Canceled)

22. (Currently amended) A system comprising:

a sample rate converter configured to receive a first input digital data stream and a second input digital data stream and to convert each of the first and second input digital data streams from corresponding input sample rates to a predetermined output sample rate;

wherein the sample rate converter includes:

a clock source,

a first counter coupled to receive a clock signal from the clock source and configured to count cycles of the clock signal in a sample period of the first input digital data stream,

a second counter coupled to receive the clock signal from the clock source and configured to count cycles of the clock signal in a sample period of the second input digital data stream, and

a data processor coupled to the first and second counters and configured to

read a first number of cycles counted by the first counter and a second number of cycles counted by the second counter,

estimate a first input sample rate of the first input digital data stream,

calculate a second input sample rate of the second input digital data stream by multiplying the first input sample rate by the ratio of the second number of cycles to the first number of cycles, and

convert each of the first and second input digital data streams from the corresponding input sample rates to the predetermined output sample rate.

23. (Canceled)

24. (Previously presented) The system of claim 22, wherein the first and second input sample rates are not restricted to a set of predetermined sample rates.

25. (Previously presented) The system of claim 24, wherein the first and second input sample rates are different.

26. (Previously presented) The system of claim 22, further comprising one or more low-pass filters configured to filter the first number of cycles and the second number of cycles.

27. (Previously presented) The system of claim 22, wherein the data processor is configured to reset the first and second counters each time a succeeding frame sync signal is received.

28. (Currently amended) The system of claim [[1]] 2, wherein the data processor is configured to convert the first input digital data stream from the first input sample rate to the predetermined output sample rate in a first channel, wherein the data processor is configured to convert the second input digital data stream from the second input sample rate to the predetermined output sample rate in a second channel, and wherein wherein at least a portion of a plurality of processing components of the first and second channels are common to both the first and second channels.

29. (Previously presented) The system of claim 22, further comprising a first FIFO and a second FIFO, wherein data from the first digital data stream is stored in the first FIFO and data from the second digital data stream is stored in the second FIFO.

30. (Previously presented) The system of claim 22, wherein the sample rate converter is implemented in a pulse-width modulated digital audio amplifier.

31. (Currently amended) A method comprising:

receiving a clock signal from a clock source;

receiving a first input digital data stream;

receiving a second input digital data stream;

counting a first number of cycles of the clock signal in a sample period of the first input digital data stream and a second number of cycles of the clock signal in a sample period of the second input digital data stream;

estimating a first input sample rate of the first input digital data stream[[,]];

calculating a second input sample rate of the second input digital data stream by multiplying the first input sample rate by the ratio of the second number of cycles to the first number of cycles, and

converting each of the first and second input digital data streams from the corresponding input sample rates to a predetermined output sample rate.

32. (Canceled)

33. (Previously presented) The method of claim 31, further comprising resetting the first and second counters each time a succeeding frame sync signal is received.

34. (Previously presented) The method of claim 31, further comprising storing data from the first input digital data stream in a first FIFO and storing data from the second input digital data stream in a second FIFO.

35. (Previously presented) The method of claim 31, further comprising low-pass filtering the first number of cycles and the second number of cycles.

36. (Previously presented) The method of claim 31, wherein the first and second input sample rates are not restricted to a set of predetermined sample rates.

37. (Previously presented) The method of claim 31, wherein the first and second input sample rates are different.

38. (Previously presented) The method of claim 31, wherein the method is implemented in a pulse-width modulated digital audio amplifier.